15. (Original) The system as recited in claim 1 further comprising a voltage regulator module, the voltage regulator module including the voltage regulator circuit.

16. (Cancelled)

17. (Original) The system as recited in claim 1, wherein the decoupling capacitors are surface mounted capacitors.

18 – 34. (Cancelled)

REMARKS

Claims 1, 4-9, 11, 13, 15 and 17 are currently pending in the application. Claims 1 and 11 have been amended, while claim 2 has been cancelled.

Claim Objection:

Claim 11 has been amended to comply with formal requirements.

Objection to the Drawings:

The drawings were objected to. In particular, the Office Action states that the cross-hatching of the IC, the power laminate, and PCB in Figures 1-6 is improper. Applicant has amended the drawings and attached herewith a request for drawing changes. Applicant submits that the drawings are properly crosshatched. For example, in Figure 1, IC 5 is crosshatched as Heat or Cold Insulation, which is consistent with ceramic material that is used for external packaging of many integrated circuits. PCB 15 and Power Laminate 20 of Figure 1 are crosshatched as Sections of Synthetic Resin or Plastic, which is consistent with fiberglass and/or other dielectric material(s) used in the construction of printed circuit boards and other laminated structures. Applicant submits that the drawings meet the crosshatching requirements illustrated in MPEP 608.02. Accordingly, approval of the drawings is respectfully requested.

35 U.S.C. § 103 Rejection:

Claims 1-2, 4-9, 13, 15, and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Feilchenfeld et al, U.S. Patent 5,798,563 (hereafter 'Fed'), in view of Smith et al, U.S. Patent 5,695,297. Applicant respectfully traverses this rejection.

The cited references, taken singly or in combination, do not teach or suggest all of the features of the independent claims. Fed teaches an organic chip carrier particularly useful with flip chips, comprising an organic dielectric layer, a first layer of circuitry disposed on the dielectric layer, an organic conformational coating disposed over the first layer of dielectric and the first layer of circuitry, and a layer of fine line circuitry having line width of about 2.0 mil or less, preferably about 1.0 mil or less, preferably about 0.7 mil, and a space between lines of about 1.5 mil or less, preferably about 1.1 mil or less, disposed on the conformational layer. Preferably the dielectric layer is free of woven fiber glass. The conformational coating preferably has a dielectric constant of about 1.5 to about 3.5, and a percent planarization of greater than about 3.5%.

Smith teaches a mounting structure for providing DC power to an IC package. The mounting structure comprises a socket for receiving an IC package, having one or more IC chips, and a power supply for supplying at least one specified DC voltage to the IC package. The power supply is coupled to the IC package by conductive paths formed in the socket.

In contrast, Applicant teaches a power laminate for providing core power to an integrated circuit. Independent claim 1 recites, in pertinent part:

> "a printed circuit board (PCB) including at least one signal layer for conveying signals to and from the integrated circuit, wherein the PCB is not configured for providing core power to the integrated circuit;
>
> a power laminate for providing core power to the integrated circuit ... wherein the power laminate is separate from the PCB" (Emphasis added)

Neither Fed nor Smith teach or suggest the combination of features recited in the independent claim. Applicant can find no teaching or suggestion in the cited references (whether taken singly or in combination) of a system having a power laminate for providing core power to the integrated circuit and a PCB that is not configured for providing core power to the integrated circuit.

In rejecting claim 1, the Examiner refers to carrier 10 of Figures 1 and 2 of Fed as a power laminate. In rejecting claim 2 (which has since been cancelled and its features incorporated into currently amended claim 1), the Examiner refers to carrier 10 of Figures 1 and 2 as a PCB. Applicant submits that the power laminate and the PCB as recited in claim 1 are different and separate entities. Applicant further submits that Fed provides no teaching as to the respective roles of the carrier 10 and substrate 46 in providing core power to an integrated circuit.

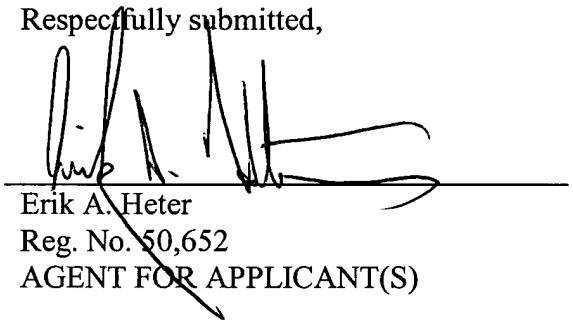
In light of the above remarks, Applicant submits that the standard for obviousness has not been met. Accordingly, removal of the 35 U.S.C. § 103(a) rejection is respectfully requested.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5181-71501/BNK.

Respectfully submitted,



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Date: 10/30/03